



# C2M0040120D

## Silicon Carbide Power MOSFET Z-FET™ MOSFET

N-Channel Enhancement Mode

### Features

- High Speed Switching with Low Capacitances
- High Blocking Voltage with Low  $R_{DS(on)}$
- Easy to Parallel and Simple to Drive
- Resistant to Latch-Up
- Halogen Free, RoHS Compliant

### Benefits

- Higher System Efficiency
- Increased System Switching Frequency
- Reduced Cooling Requirements
- Increased System Reliability

### Applications

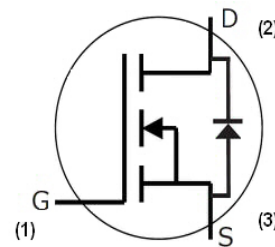
- Solar Inverters
- Switch Mode Power Supplies
- High Voltage DC/DC converters
- Motor Drive

$V_{DS}$	1200 V
$I_D @ 25^\circ C$	60 A
$R_{DS(on)}$	40 m $\Omega$

### Package



TO-247-3



Part Number	Package
C2M0040120D	TO-247-3

### Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
$I_{DS(DC)}$	Continuous Drain Current	60	A	$V_{GS} = 20 V, T_C = 25^\circ C$	Fig. 19
		40		$V_{GS} = 20 V, T_C = 100^\circ C$	
$I_{DS(pulse)}$	Pulsed Drain Current	160	A	Pulse width $t_p$ limited by $T_{jmax}$ $T_C = 25^\circ C$	Fig. 22
$V_{GS}$	Gate Source Voltage	-10/+25	V		
$P_{tot}$	Power Dissipation	330	W	$T_C=25^\circ C, T_J = 150^\circ C$	Fig. 20
$T_J, T_{stg}$	Operating Junction and Storage Temperature	-55 to +150	$^\circ C$		
$T_L$	Solder Temperature	260	$^\circ C$	1.6 mm (0.063") from case for 10s	
$M_d$	Mounting Torque	1 8.8	Nm lbf-in	M3 or 6-32 screw	



## Electrical Characteristics (T<sub>C</sub> = 25 °C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	1200			V	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 50 μA	
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.4	2.8		V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10mA	Fig. 11
		1.8	2.0		V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10mA, T <sub>J</sub> = 150 °C	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current		1	100	μA	V <sub>DS</sub> = 1200 V, V <sub>GS</sub> = 0 V	
I <sub>GSS</sub>	Gate-Source Leakage Current			250	nA	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V	
R <sub>DS(on)</sub>	Drain-Source On-State Resistance		40	52	mΩ	V <sub>GS</sub> = 20 V, I <sub>D</sub> = 40 A	Fig. 4,5,6
			84	100		V <sub>GS</sub> = 20 V, I <sub>D</sub> = 40 A, T <sub>J</sub> = 150 °C	
g <sub>fs</sub>	Transconductance		15.1		S	V <sub>DS</sub> = 20 V, I <sub>DS</sub> = 40 A	Fig. 7
			13.2			V <sub>DS</sub> = 20 V, I <sub>DS</sub> = 40 A, T <sub>J</sub> = 150 °C	
C <sub>iss</sub>	Input Capacitance		1893		pF	V <sub>GS</sub> = 0 V V <sub>DS</sub> = 1000 V f = 1 MHz	Fig. 17,18
C <sub>oss</sub>	Output Capacitance		150				
C <sub>rss</sub>	Reverse Transfer Capacitance		10				
E <sub>oss</sub>	C <sub>oss</sub> Stored Energy		82				μJ
t <sub>d(on)</sub>	Turn-On Delay Time		14.8		ns	V <sub>DD</sub> = 800 V, V <sub>GS</sub> = -5/20 V I <sub>D</sub> = 40 A, R <sub>G(ext)</sub> = 2.5 Ω, R <sub>L</sub> = 16 Ω Timing relative to V <sub>DS</sub> Per IEC60747-8-4 pg 83	Fig. 27
t <sub>r</sub>	Rise Time		52				
t <sub>d(off)</sub>	Turn-Off Delay Time		26.4				
t <sub>f</sub>	Fall Time		34.4				
E <sub>ON</sub>	Turn-On Switching Loss		1.0		mJ	V <sub>DS</sub> = 800 V, V <sub>GS</sub> = -5/20 V, I <sub>D</sub> = 40A, R <sub>G(ext)</sub> = 2.5Ω, L = 80 μH	Fig. 25
E <sub>OFF</sub>	Turn Off Switching Loss		0.4				
R <sub>G</sub>	Internal Gate Resistance		1.8		Ω	f = 1 MHz, V <sub>AC</sub> = 25 mV, ESR of C <sub>ISS</sub>	

## Built-in SiC Body Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V <sub>SD</sub>	Diode Forward Voltage	3.6		V	V <sub>GS</sub> = -5 V, I <sub>SD</sub> = 20 A, T <sub>J</sub> = 25 °C	Note 1
		3.3		V	V <sub>GS</sub> = -5 V, I <sub>SD</sub> = 20 A, T <sub>J</sub> = 150 °C	
t <sub>rr</sub>	Reverse Recover time	54		ns	V <sub>GS</sub> = -5 V, I <sub>SD</sub> = 40 A T <sub>J</sub> = 25 °C VR = 800 V dif/dt = 1000 A/μs	Note 1
Q <sub>rr</sub>	Reverse Recovery Charge	283		nC		
I <sub>rrm</sub>	Peak Reverse Recovery Current	15		A		

Note (1): When using SiC Body Diode the maximum recommended V<sub>GS</sub> = -5V

## Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
R <sub>θJC</sub>	Thermal Resistance from Junction to Case	0.34	0.38	°C/W		Fig. 21
R <sub>θJA</sub>	Thermal Resistance from Junction to Ambient		40			

## Gate Charge Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
Q <sub>gs</sub>	Gate to Source Charge	28		nC	V <sub>DS</sub> = 800 V, V <sub>GS</sub> = -5/20 V I <sub>D</sub> = 40 A Per IEC60747-8-4 pg 21	Fig. 12
Q <sub>gd</sub>	Gate to Drain Charge	37				
Q <sub>g</sub>	Gate Charge Total	115				

## Typical Performance

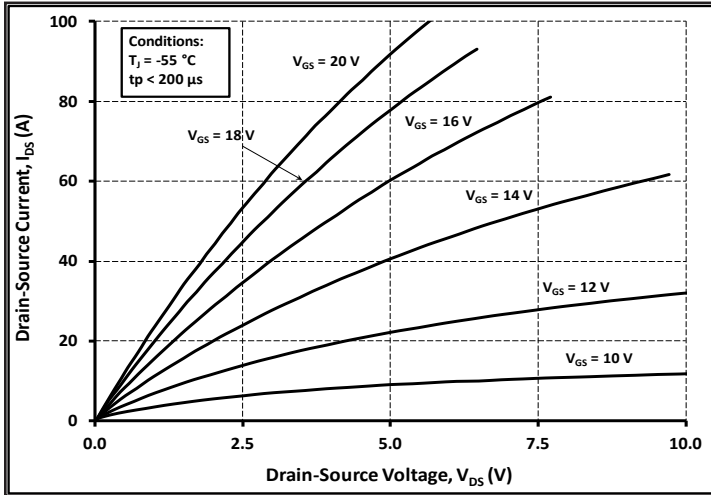


Figure 1. Typical Output Characteristics  $T_j = -55\text{ }^\circ\text{C}$

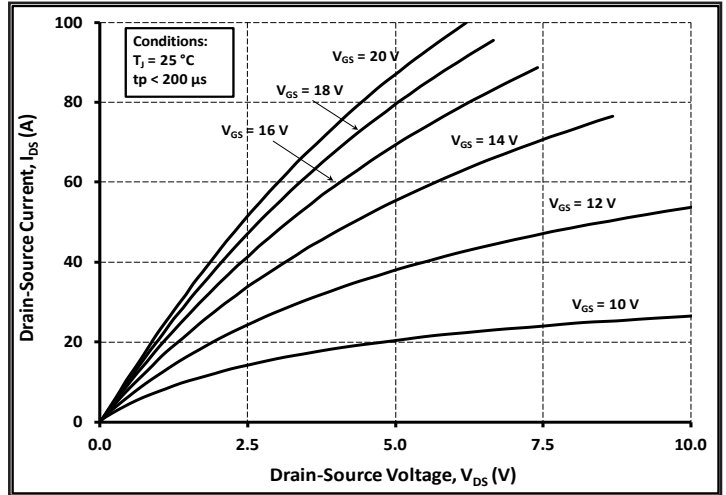


Figure 2. Typical Output Characteristics  $T_j = 25\text{ }^\circ\text{C}$

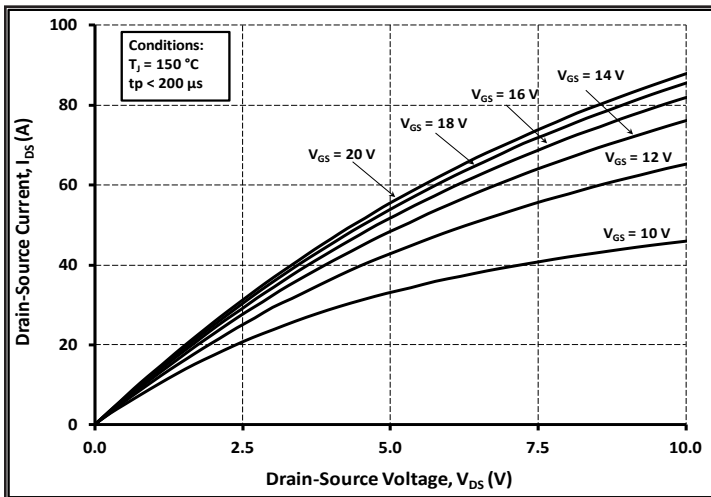


Figure 3. Typical Output Characteristics  $T_j = 150\text{ }^\circ\text{C}$

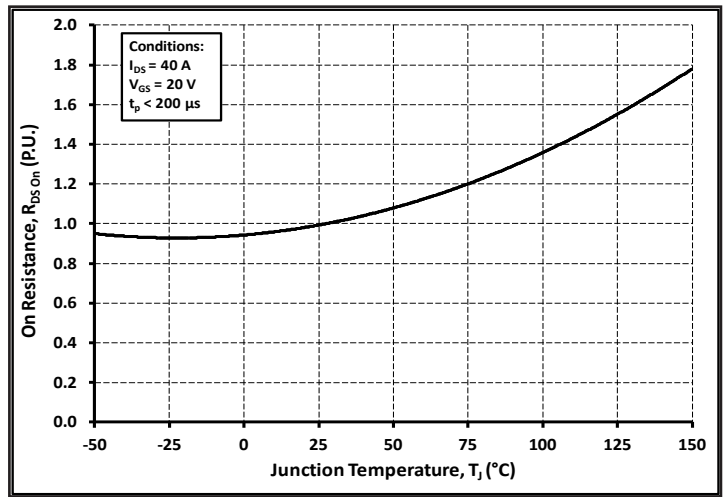


Figure 4. Normalized On-Resistance vs. Temperature

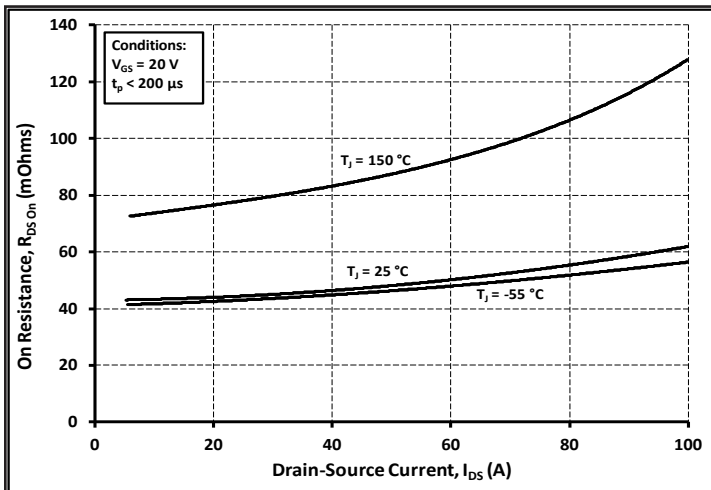


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

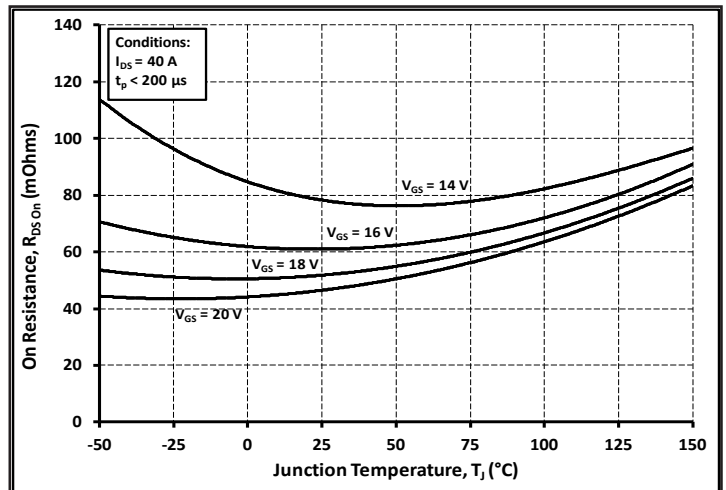


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage

# Typical Performance

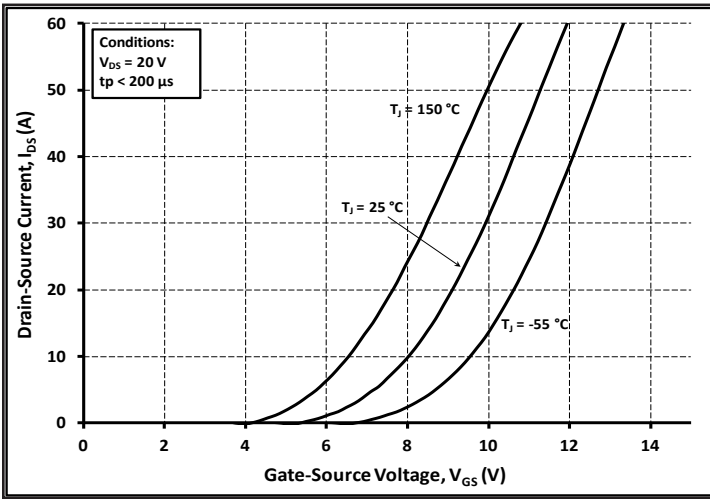


Figure 7. Typical Transfer Characteristic For Various Temperatures

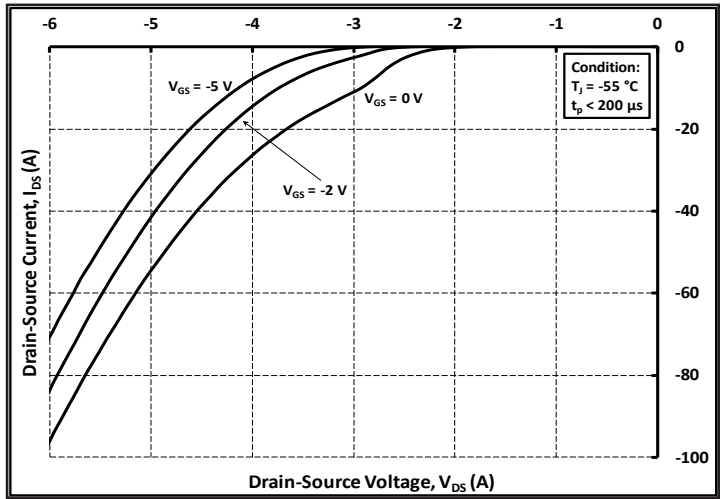


Figure 8. Typical Body Diode Characteristic  $T_J = -55\text{ }^\circ\text{C}$

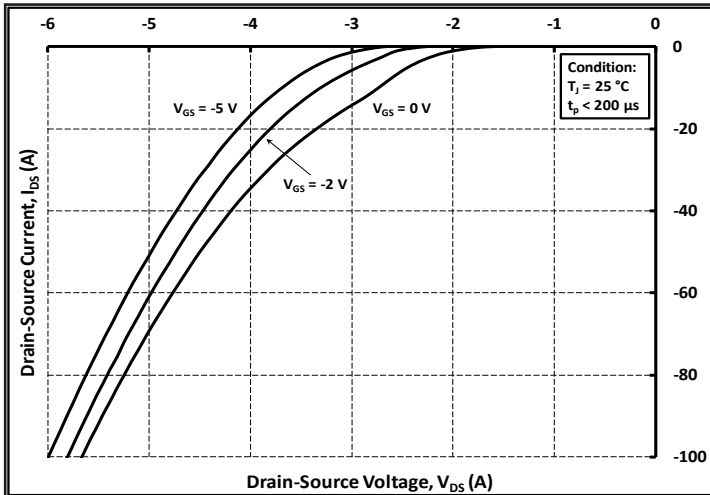


Figure 9. Typical Body Diode Characteristic  $T_J = 25\text{ }^\circ\text{C}$

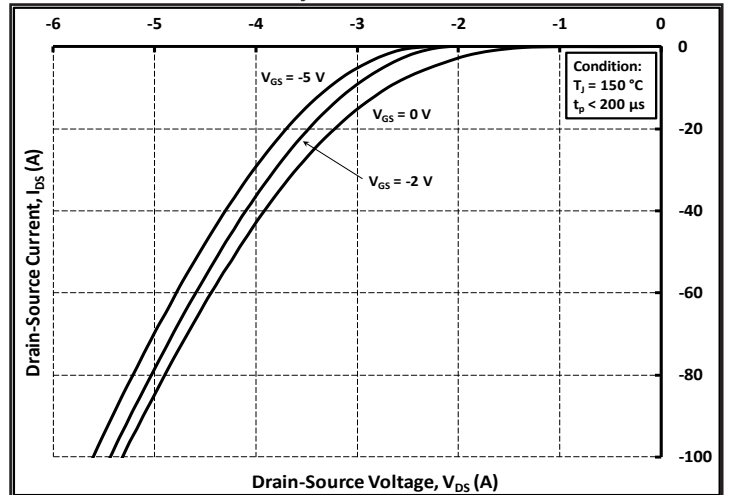


Figure 10. Typical Body Diode Characteristic  $T_J = 150\text{ }^\circ\text{C}$

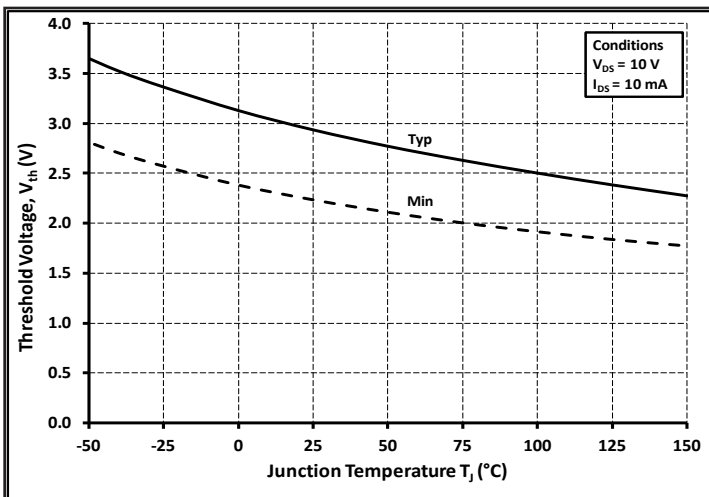


Figure 11. Typical and Minimum Threshold Voltage vs. Temperature

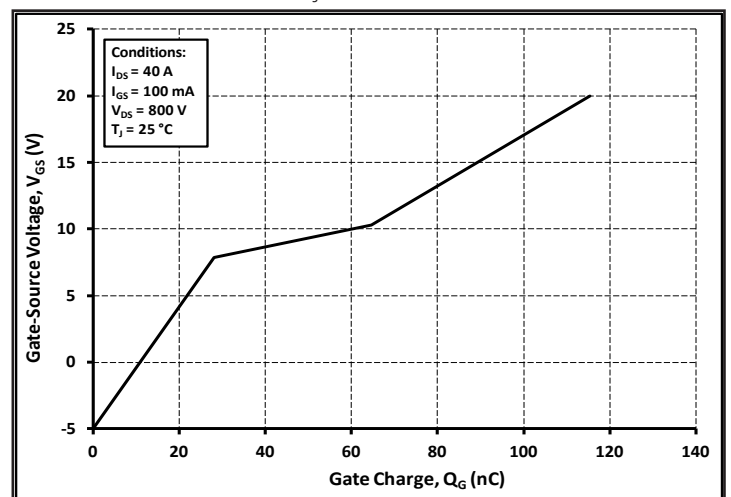


Figure 12. Typical Gate Charge Characteristic 25 °C

## Typical Performance

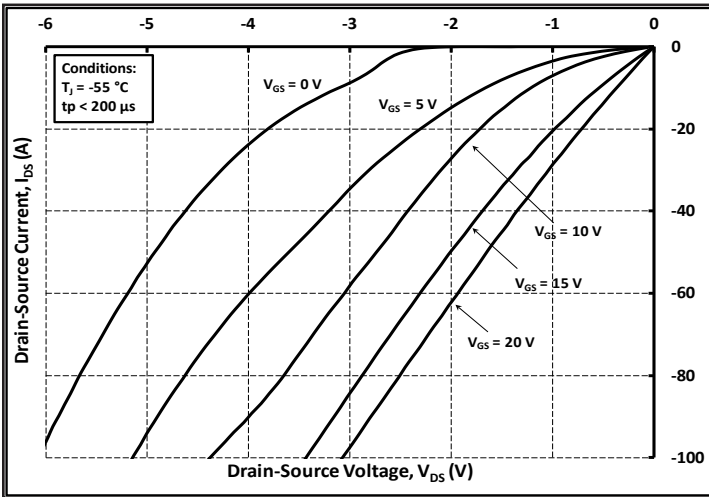


Figure 13. Typical 3rd Quadrant Characteristic  
 $T_j = -55\text{ }^\circ\text{C}$

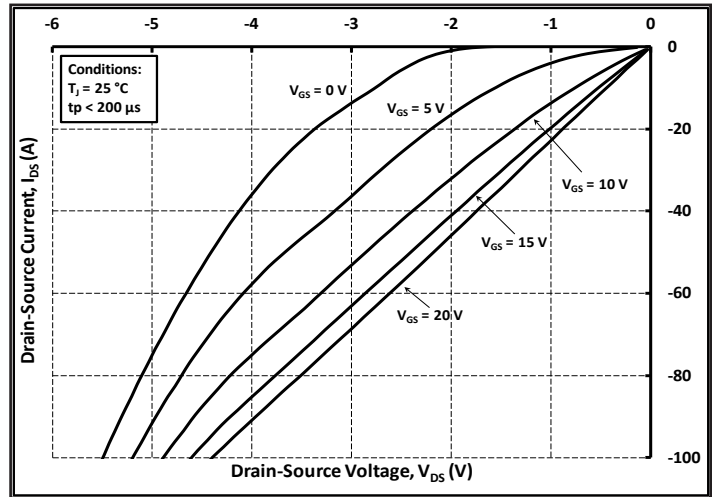


Figure 14. Typical 3rd Quadrant Characteristic  
 $T_j = 25\text{ }^\circ\text{C}$

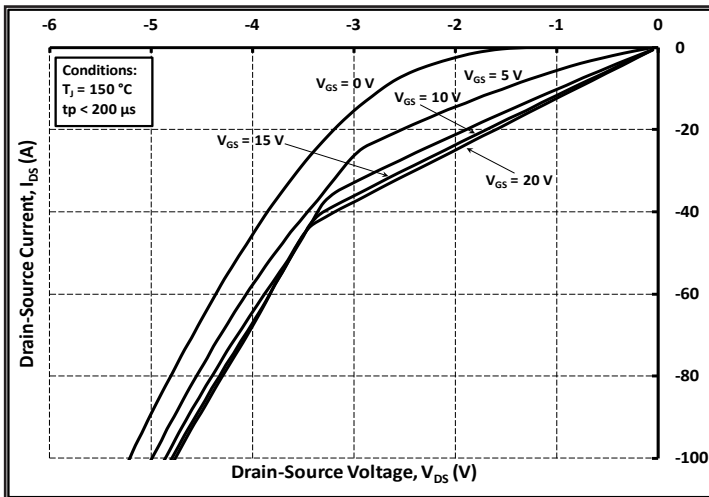


Figure 15. Typical 3rd Quadrant Characteristic  
 $T_j = 150\text{ }^\circ\text{C}$

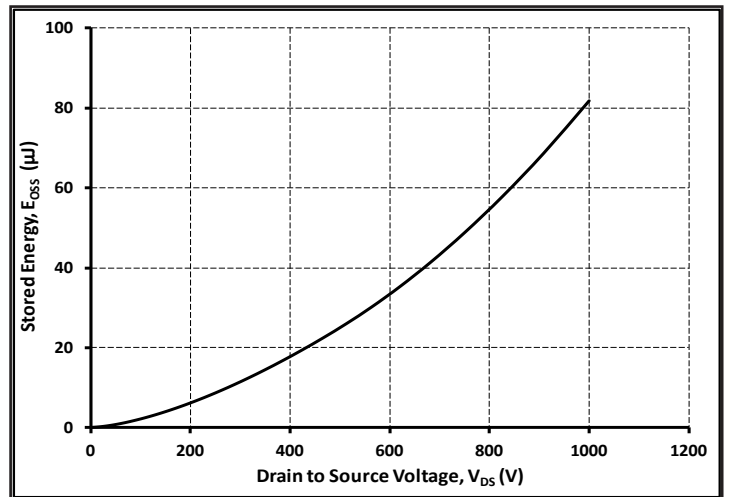


Figure 16. Typical Output Capacitor Stored Energy

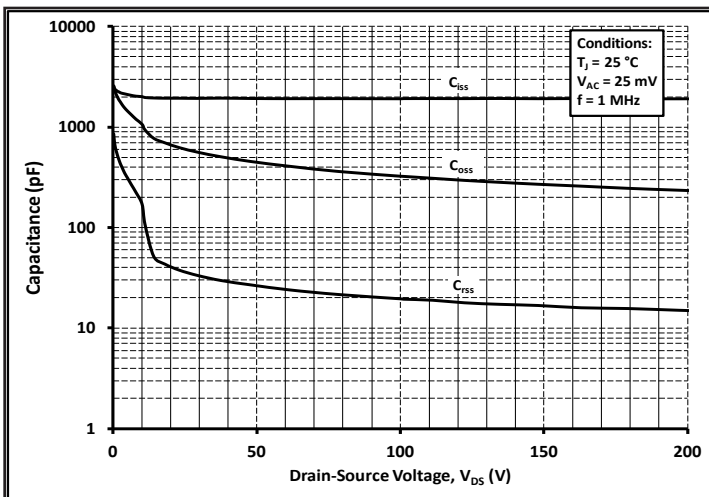


Figure 17. Typical Capacitances vs Drain Voltage  
(0-200 V)

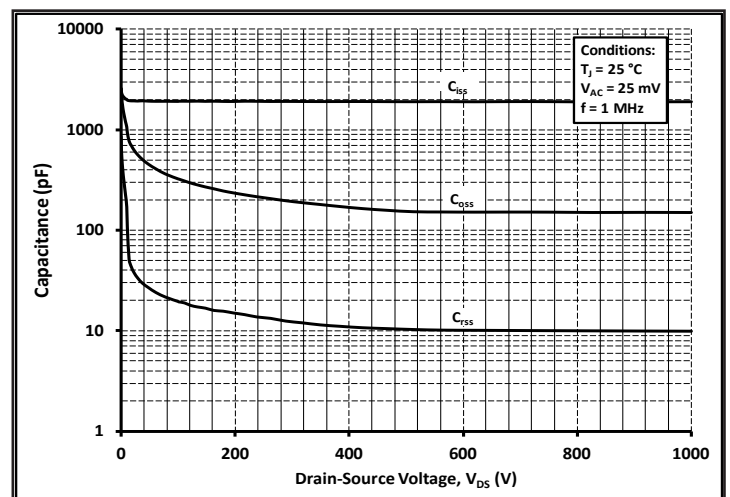


Figure 18. Typical Capacitances vs Drain Voltage  
(0-1000 V)

## Typical Performance

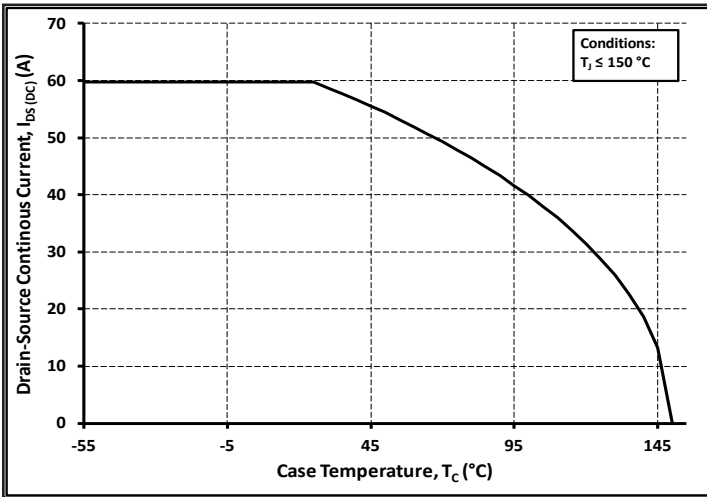


Figure 19. Continuous  $I_{DS}$  Current derating curve

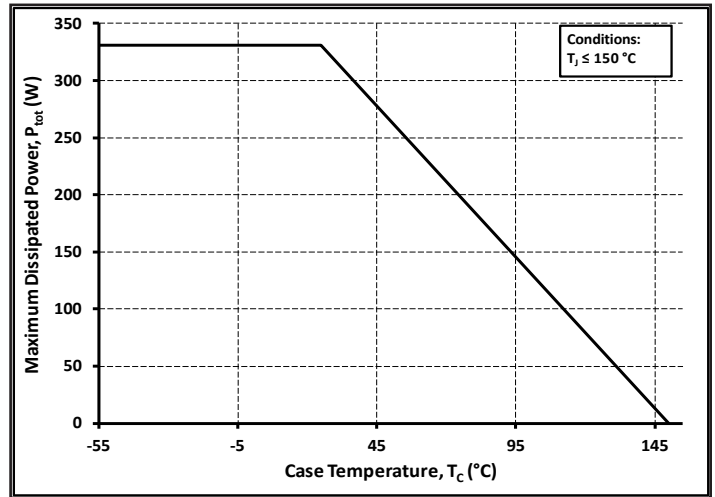


Figure 20. Power Dissipation Derating Curve

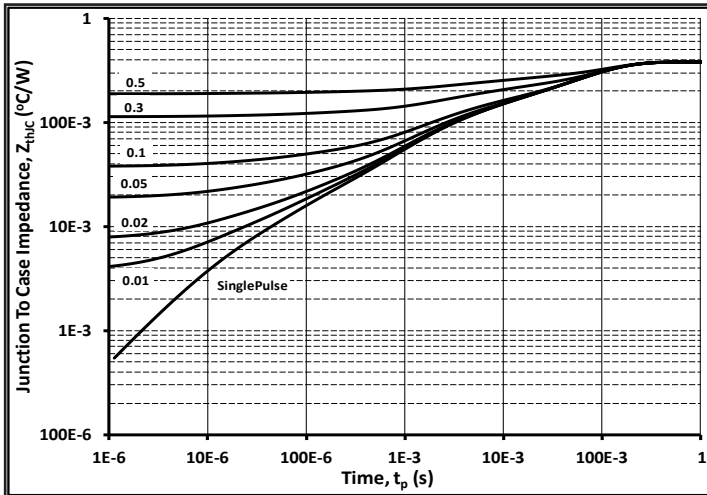


Figure 21. Typical Transient Thermal Impedance (Junction - Case) with Duty Cycle

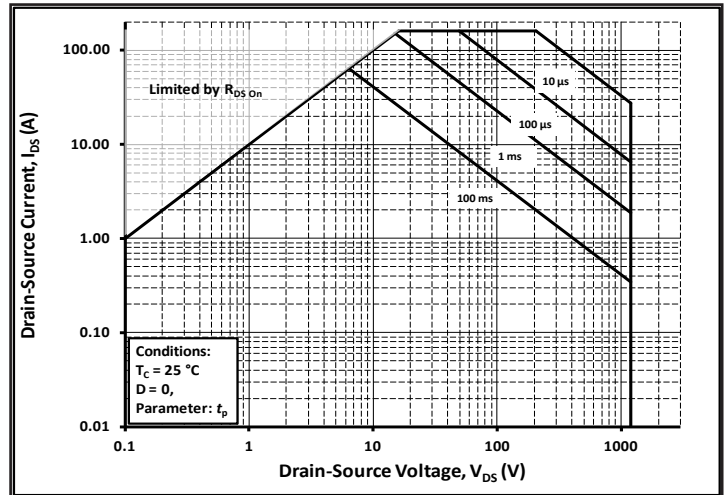


Figure 22. Safe Operating Area

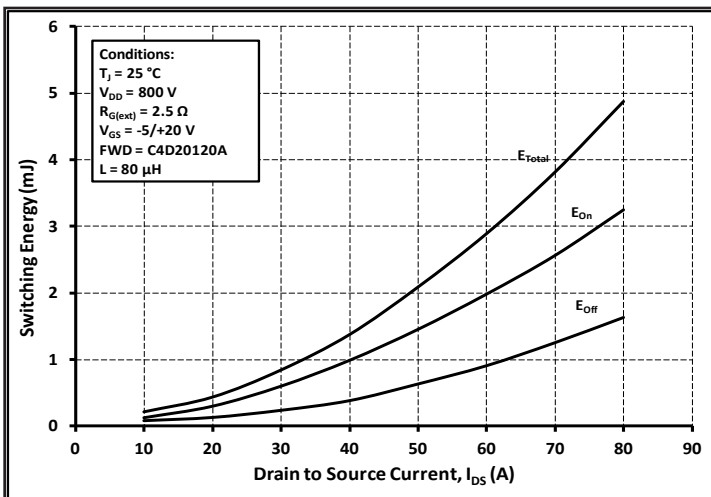


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 800V$ )

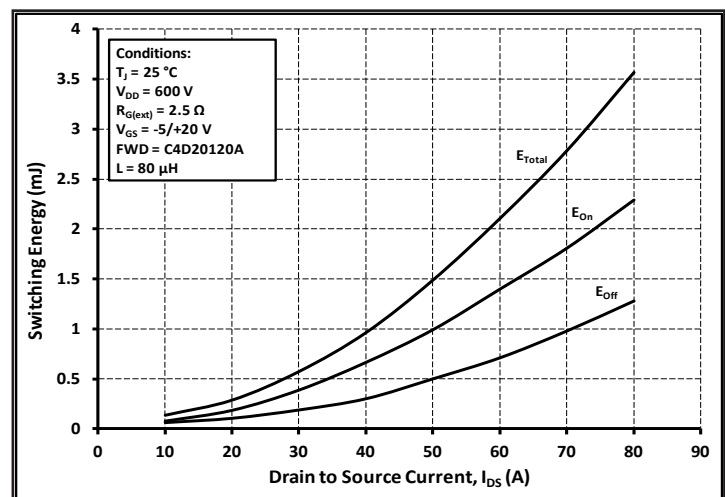


Figure 24. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 600V$ )

## Typical Performance

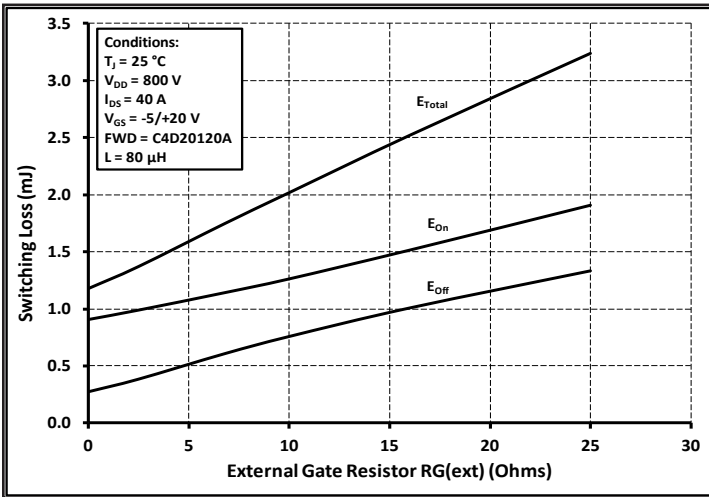


Figure 25. Clamped Inductive Switching Energy vs.  $R_{G(ext)}$

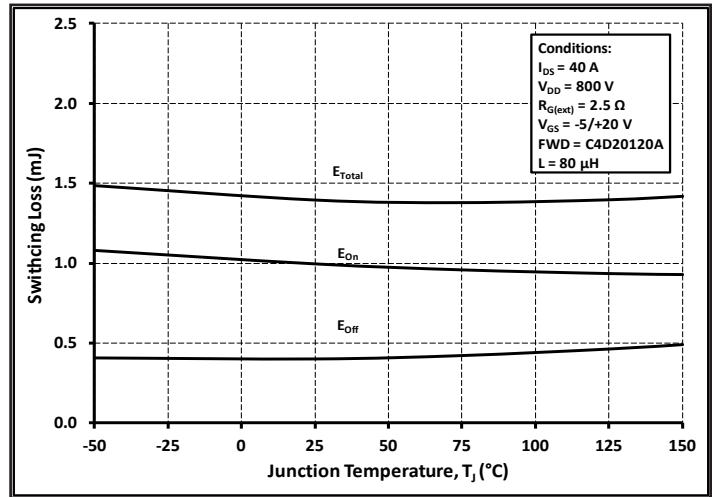


Figure 26. Clamped Inductive Switching Energy vs. Junction Temperature

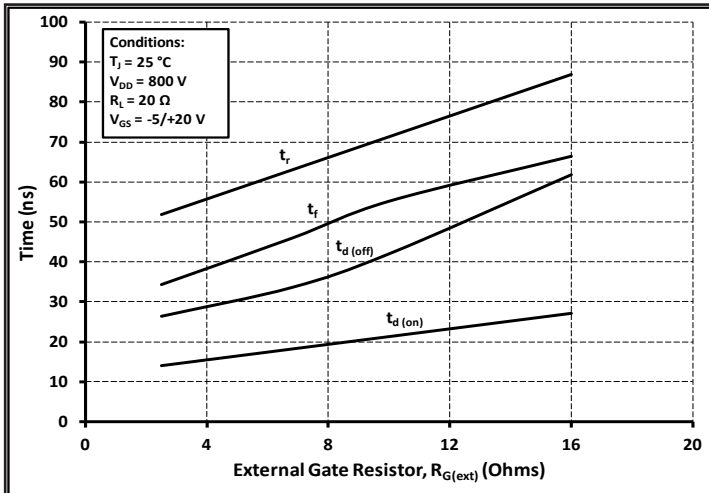


Figure 27. Resistive Switching Times vs. External Gate Resistor ( $V_{DD} = 800\text{ V}$ ,  $I_D = 40\text{ A}$ )

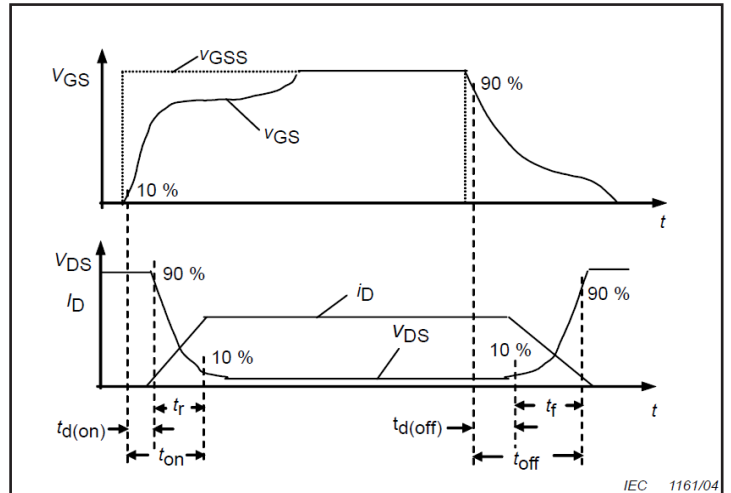


Figure 28. Resistive Switching Time Description

## Test Circuit Schematic

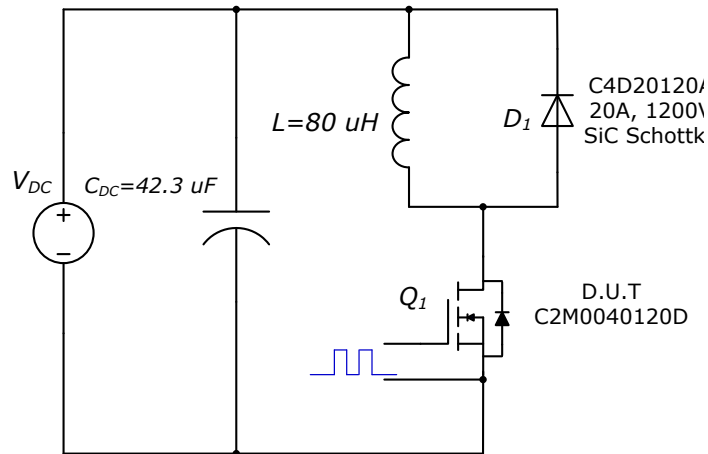


Figure 30. Clamped Inductive Switching Waveform Test Circuit

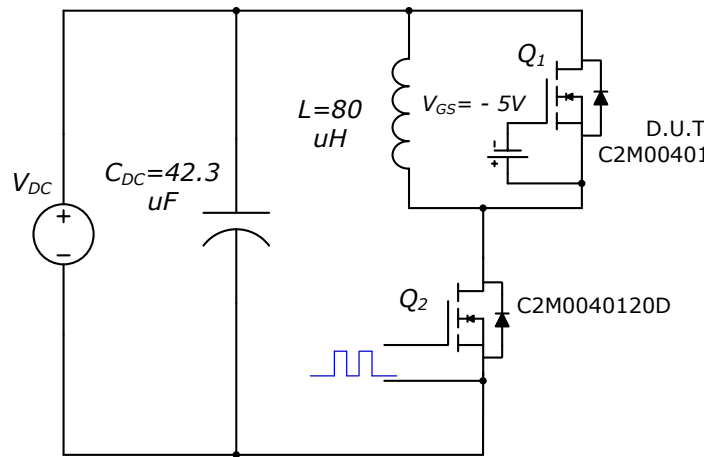


Figure 31. Body Diode Recovery Test Circuit

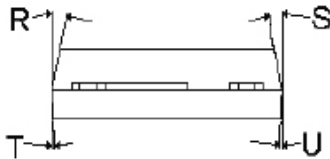
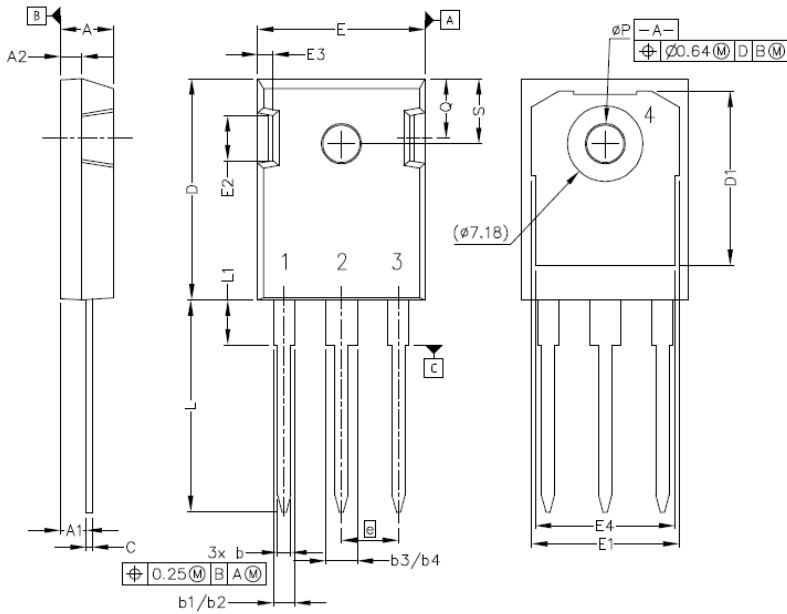
## ESD Ratings

ESD Test	Total Devices Sampled	Resulting Classification
ESD-HBM	All Devices Passed 1000V	2 (>2000V)
ESD-MM	All Devices Passed 400V	C (>400V)
ESD-CDM	All Devices Passed 1000V	IV (>1000V)



## Package Dimensions

Package TO-247-3

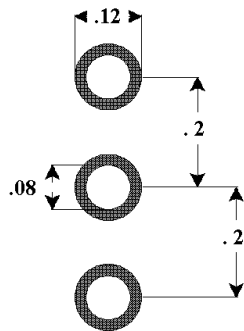


Pinout Information:

- Pin 1 = Gate
- Pin 2, 4 = Drain
- Pin 3 = Source

POS	Inches		Millimeters	
	Min	Max	Min	Max
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.042	.052	1.07	1.33
b1	.075	.095	1.91	2.41
b2	.075	.085	1.91	2.16
b3	.113	.133	2.87	3.38
b4	.113	.123	2.87	3.13
c	.022	.027	0.55	0.68
D	.819	.831	20.80	21.10
D1	.640	.695	16.25	17.65
D2	.037	.049	0.95	1.25
E	.620	.635	15.75	16.13
E1	.516	.557	13.10	14.15
E2	.145	.201	3.68	5.10
E3	.039	.075	1.00	1.90
E4	.487	.529	12.38	13.43
e	.214 BSC		5.44 BSC	
N	3		3	
L	.780	.800	19.81	20.32
L1	.161	.173	4.10	4.40
$\phi P$	.138	.144	3.51	3.65
Q	.216	.236	5.49	6.00
S	.238	.248	6.04	6.30

## Recommended Solder Pad Layout



TO-247-3

Part Number	Package	Marking
C2M0040120D	TO-247-3	C2M0040120



## Notes

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- **RoHS Compliance**

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Cree representative or from the Product Documentation sections of [www.cree.com](http://www.cree.com).

- **REACH Compliance**

REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact a Cree representative to insure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, air traffic control systems.